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# A Novel Designing of Controlled Buffer Register using Single Electron Transistor Modelling

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**Abstract**
*Rapid progress in fabrication technology of silicon nano-devices has shrunk the device dimension toward 10nm scale. With this continuous device downscaling technique the mainstream CMOS technology has reached its fundamental physical limits. Consequently this has imparted detrimental effects that play an escalating role leading to a difficult and costly miniaturization of MOSFETs and even more to a future end of the classic scaling. In such context a serious aspirant for the next generation electronics were required; anticipating that it should be potentially capable to overcome the limitation of the existing technology. Single electronics technology (SET), a new field of solid state science and technology then after have evolved speedily in both theory and experiments because the essential nanofabrication techniques have become available during the past two decades. Now a group of researchers has initiated to incorporate SET in logic device designing in digital electronics. Here the authors investigate the probability of using SET logic circuit in Controlled Buffer Register design so that such architectures can show new direction with greater proximity in the line of adaptability for mass production of SETs.*

**Keywords**
*Single Electronic Transistor, Coulomb Blockade, Tunneling Effect, Controlled Buffer Register and Giga Scaled ICs.*

## I. Introduction

Next generation Giga-scale ICs will confine themselves in fewer electrons in device action so that power consumption and battery voltage may be reduced. This is quite complicated to achieve in conventional devices owing to statistical fluctuations resulting in noise. The dominating limiting factors projected up till now includes but are not restricted to are - (1) material and processing related limitation (doping fluctuation, avalanche break down, MOS interface instability, electro-migration, stress-migration, interface reaction), (2) power limitation, (3) wiring limitation, (4) quantum mechanical limitation (quantum fluctuation. failure of device and device isolation due to tunnelling) and (5) system architecture limitation. These determining factors enunciated the search of novel technologies which ended with the invention of SET [1-5].

The exploitation of single electrons was demonstrated empirically in the determining experiments by Millikan in 1911, but in solid state circuit designs it was not executed until the late 1980s, despite some important earlier background works [6-8]. The SET made single-electron device (SED) attracted lot of attention for future large-scale integration because of its low-power nature, small size and allowance of manipulation of Individual electrons. Single electronics make use of the available possibility and control the movement and position of a single electron or a small number of electrons. The elementary principle of single electronics is the Coulomb blockade, first observed and studied by Gorter [9]. SEDs make use of the Coulomb blockade (CB), which occurs in tiny structures made from conductive material due to the electrostatic interactions of confined electrons. The development of Coulomb blockade, single-electron tunnelling and related phenomena from the physical point of view have been observed in semiconductor single-electron transistors, metallic nanostructure devices, low-dimensional organic nanostructures, and III–V compound semiconductors etc.

The computational methodology adapted in designing low power complex SET structures involves not only robust fabrication but also includes rigorous study of logical understanding of device fundamentals. This creates enormous scope of inventing modernised new dimensional SED structures having all intrinsic merits of next generation devices. One such attempt has been reported here.

### 1. The Unique Potentialities of SET

A single electron, structurally, is sufficient enough to store information. If a single electron is present in the input signal then information is present else there is no information. For SED function representation using logical synthesis like NOT, NOR, AND, NAND, X-OR merely takes 4ns for propagation delay while for CMOS gates the same device takes 12ns. Thus, the execution time reduces to about one third to that of conventional logic based circuit and hence the efficiency in terms of speed is enhanced to 300% i.e., nearly equal to electronic speed. One distinguishing merit is that in complex conventional circuit, component(s) cannot be reduced whereas in single electron circuit nodes can be reduced, eventually circuit becomes more faster. SET circuit has advantages of reducing the power consumption as a single electron is sufficient to store information, which is not in the case of CMOS circuits. The instability and reliability problem is controlled by extremely low power operation. Also the speed power product is predicted to lie close to the quantum limit set by the Heisenberg's uncertainty principle. SEDs are confined in a small space so that the integration density is higher than the CMOS based VLSI / ULSI level. It was empirically demonstrated that the executive sensitivity is about 3 orders of magnitude which is greater than the conventional solid-state MOSFET. The instigating feature of SET is the generality and robustness of the effect and the relative simplicity of the device structures; it makes the single-electronics the most likely candidate for future ultra dense digital circuits. Furthermore, the noise during operation is ultra-low for single electron device(s) [10-12].

### 2. Structural View of SET

All SETs can be made by placing two tunnel junctions in series. The two tunnel junctions craft the "Coulomb island" where electrons

can only enter by tunnelling through one of the insulators. The device consists of three terminals very much similar to CMOS transistors: the outside terminal of each tunnel junction, and a "gate" terminal which is capacitively coupled to the node amid the two tunnel junctions. The capacitor acts as a third tunnel junction, however, it is much thicker than the others so that no electrons can tunnel through it. The capacitor here resembles a way of setting the electric charge on the Coulomb island [13].

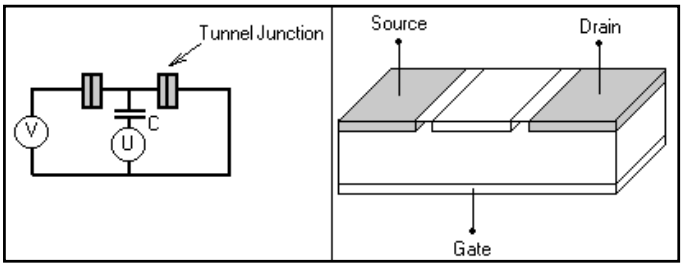


Fig. 1: A detailed view of two Tunnel Junctions in series of Single Electron Transistor

The prior conditions for successful tunnelling are that when the gate voltage is set to zero, very little tunnelling occurs in the course of the two tunnel junctions [Fig.-1]. This phenomenon of opposition to tunnelling is called the Coulomb blockade. Considerably if the gate voltage is raised to e/2C it corresponds to half of the charge of an electron on the plates of the gate capacitor; next the tunnelling current rises dramatically. This SET is used in the memory chip

### (i). SET in Logical Milieu

The Single electron based logic gates have been reported in different research publications based on binary decision diagram (BDD) with clock pulses of 1ns each [14,15]. BDD has been widely used for design verification also. The technique of tunnelling of an electron is utilized for those gates remain the same as shown in Fig.-2.

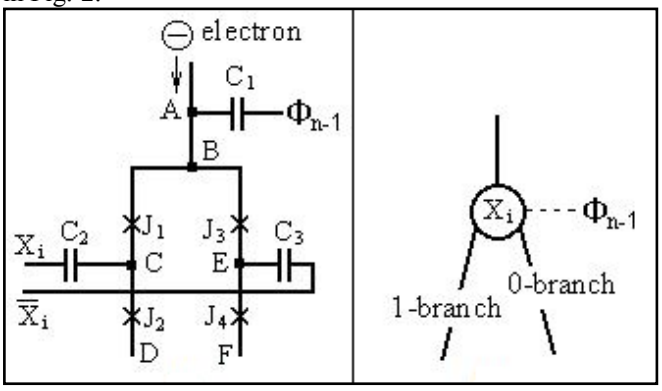


Fig. 2: Root Node Representation of Single Electron Circuit

The root node as illustrated in Fig.-2 (along with the symbol of root node) is controlled by a signal $X_i$ and a clock pulse $\Phi_{n-1}$, n=1, 2…. It comprises of four tunnel junctions ($J_1$, $J_2$, $J_3$ and, $J_4$) besides three capacitances ($C_1$, $C_2$ and $C_3$). The condition is if an electron comes at point A and pulse $\Phi_{n-1}$>5mV is applied then the electron can cross tunnel junctions ($J_1$ and $J_3$) to C or (E) based on whether the Coulomb energy [$E_c=e^2/(2C)$] plus applied energy is greater than the potential height of the barrier energy of junction(s) $J_1$ (or $J_3$). According to this principle, the electron follows the path ABCD (or ABEF) if the signal $X_i$>5mVand the corresponding total energy (Coulomb energy + applied energy) is greater than static potential junction energy of $J_2$ (or $J_4$). Hereafter, this path ABCD (or ABEF) is denoted as 1-branch (or 0-branch).

### (ii). SET Logical Synthesis

In the threshold of low power consuming nano scaled digital electronics where people are craze for day to day latest inventions; SETs will harvest the new seeds of next generation consumer electronics in digital electronics industries. Therefore, it is high time for the researchers to ponder over new directions of fast switching, low power and less space consuming logic circuits vice conventional circuits to meet the growing demands of industries. The authors here rely on the previous work done by Gope et.al. [16-18], and Degawa et.al. [19], for logical synthesis of SET. Different conventional CMOS based gates are represented along with its SET counterpart in the Table-1 below.

Table 1: Logical Representation of the Gates

| CMOS | SET |
|---|---|
| A, B, OR Gate | |
| A, B, AND gate | |
| A, NOT | |

Combinational logic verification combines checking two Boolean networks for functional equivalence. In digital system, equivalence checking of two circuits is a catastrophic setback. Circuit behaviour alters due to technological enhancement or optimization, but the circuit has to sustain or hold the same behaviour as in before. There are many methods that have been suggested satisfactorily and quite are undoubtedly efficient. Still the search for another persists.

Thus researchers whenever intend to scale down computer chips ever smaller; the idea of incorporating SETs has become increasingly appealing. Like several other electronic devices, they uphold the potential to reach the molecular scale and would confine itself in far less space as compared to their conventional counterparts. The small size, fast in action, and low power dissipation of SET circuits make them potentially useful and best competent for next generation logic and memory circuits

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[20-22].
Based on such popular techniques the authors here demonstrate a 'Controlled Buffer Register' to exploit the utmost intrinsic qualities of SET and thereafter a comparative study is made to determine the uniqueness of SET in future nano ICs.

## III. SET based Controlled Buffer Register

Choice of designing a controlled buffer register using SET was not ambiguous. The un-put-down-able potentialities of this particular register are – (i) it allows multiple logic devices to be connected, (ii) it resolves the problem of data loss during connections, (iii) eliminates contention problem unlike other logical devices, (iv) very little scope of short circuit or permanently equivalent damage to the circuit, (v) they are available in integrated form as quad, hex or octal buffer/drivers in both uni-directional and bi-directional forms, (vi) they can be used to isolate devices and circuits from the data bus and one another. Beside these, the controlled buffer registers popularised because digital information is sent over these data buses or data highways either serially, i.e., one bit at a time, or it may be up to eight (or more) wires together in a parallel form such as in a microprocessor data bus allowing multiple tri-state buffers to be connected to the same data highway without damage or loss of data. Thus the authors believe that designing controlled buffer register was reasonable but at the same time was extremely fascinating and challenging manoeuvre [23].
Furthermore, SEDs offer a complete and concise representation for more digital functions encountered in logic-design applications [24, 25]. All such logical circuits ranging from NOT gate to CPU of a digital computer can be realized with the help of SETs. Timing analysis together with propagation delay in case of SED based digital circuits is also estimated in previous works [26]. This is why the authors being motivated by SETs here opted to design this painstaking architecture of controlled buffer register as enunciated in Fig.-3.

### (i). The Modus Operandi of the Proposed Circuit

Fig.-3 and Fig.-4 is a soft computing approach of designing of SET based controlled buffer register. Initially during $\phi_0$ the $_{CKR'}$ is LOW; the four D-F/F are correspondingly moved to RESET state. Thus at $\phi_0$ the tunnelling of electron is largely confined within the Coulomb Blockade. Now when a voltage greater than 5 mV is applied at $X_1$ and the subsequently the CLR signal is changed to HIGH state the register is initialized. Here LOAD is considered as driving force at the controlled input. When LOAD is HIGH the tunnelling phenomenon occurs; thereby the data bits (presume to be X) can reach the D inputs of F/F. Here the maximum number of electrons can tunnel through and the Coulomb Island generates no sufficient negative force to restrict the robustness of the circuit. At the positive going age of the next CLOCK pulse as shown in Fig.-4 the SET register is LOADED fully i.e., $Q_4 Q_3 Q_2 Q_1 = X_4 X_3 X_2 X_1 \Rightarrow Q = X$. This predicts the no amount of data loss occurs when the LOAD is HIGH.
When the LOAD is LOW the tunnelling of electrons is constrains which means the X-bits cannot surface to the output of F/F. Simultaneously the inverted LOAD i.e., $LOAD'$ is HIGH. As a result each F/F output is forced to feedback to its data input. Therefore the data is circulated or retained at the arrival of subsequent CLOCK pulses i.e., the contained of the SET made controlled buffer register remains unaltered in spite of varying CLOCK pulses. The same circuit can be made more complex by adding sufficient number of F/Fs.

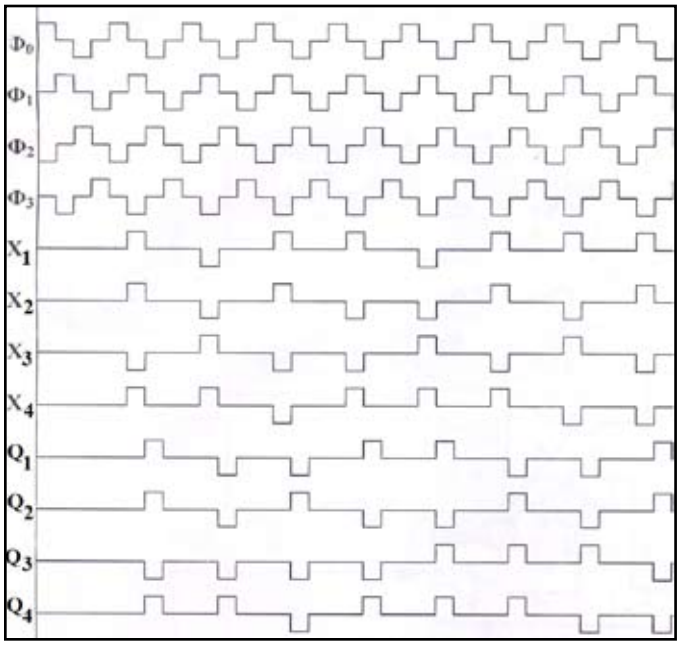

Fig. 4: Waveform of SET based controlled buffer register

### (ii). A comparative study of using CMOS & SET for designing the controlled buffer register

Table.2 correspond to the comparative study of the SET made controlled buffer register circuit considering that the most efficient fabrication technology is adapted for both CMOS based Transistor-Transistor Logic and Single Electron Transistor Logic. Moreover, in both the cases simplicity was given high attention to make the circuit cost effective. Our proposed SET based system is not only less power consuming but can obtain result at a quicker speed. Consequently, a very high-speed computation is certainly achieved with this newly proposed SET design configuration. The uniqueness lies in the fact that the power dissipation for switching a single bit is of few μW which is considerably small when compared to conventional devices. It creates higher much more component density thereby reducing the future IC sizes.

Table: 2

| Comparative study of CMOS-TTL vs SET logic gates | | | | | |
|---|---|---|---|---|---|
| Sl. No | Circuit Name | Propagation Delay time / Gate | Faster times | Power dissipation / Gate | Consume Power |
| 1 | CMOS-TTL | 12 ns | 1 | 0.01 / 10-12 mW | 1 |
| 2 | SET | 6 ns | 2 | ~1μW | 1/103 |

## IV. Conclusions

The SET as envisioned is built on the robust effects of the electronic charge discreteness. Its parallel unmatched importance has increased significantly with size reduction. In this modeling of controlled buffer register the single charge is efficiently incorporated to manipulate and control the correlated electron tunneling in small capacitance structure. Single electron device modeling research has found wide spread use in computer aided design of digital circuits. Modern era that demands superiority in consumer electronics can be achieved only if a clear and concise representation of digital functions can be obtained using SET logical synthesis which is obviously advantageous in power consumption technique and also can be adopted and if the size

can be absolutely reduced for easy portability. In this scenario SET is a fascinating technology, which explore new physical effects of charge transport. It has countless advantages over conventional CMOS technology and posses' greater figure of merit but also it has several open challenges waiting for elegant solutions. Subsequently, the logical operations create greater scope in future SET based Logic Circuits. Thus this novel approach is intended to acquire attraction in future digital electronics.

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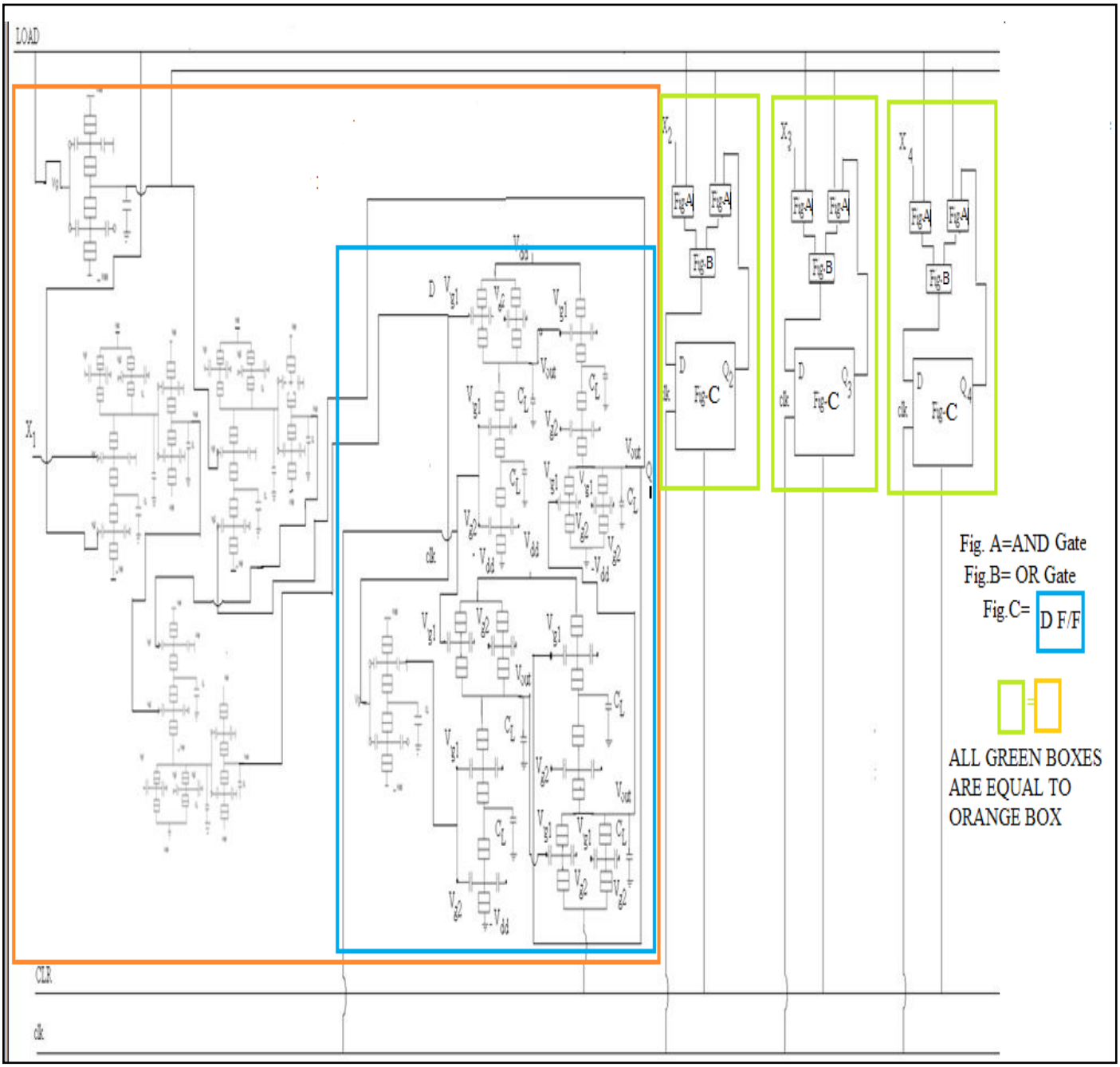


Fig. 3: SET based controlled buffer register